Study of the Dielectric Constant of Polyurethane/ Polybutyl-Methacrylate Interpenetrating Polymer Networks Using Metal–Insulator–Semiconductor Structure

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ABSTRACT: Polyurethane/polybutyl-methacrylate interpenetrating polymer networks (IPNs) film was formed on n-Si substrate by the dropping technique. When aluminum (Al) was vacuum deposited on the top of the film, the Al/IPNs/n-Si (metal–insulator–semiconductor) structure was fabricated successfully. With the aid of the high-frequency capacitance–voltage (C-V) characteristics at room temperature, the dielectric constant of IPNs was obtained. In the C-V curves, an increased hysteresis at high sweep voltage and a plateau in the depletion region were observed. This plateau indicates that the unsaturated bonds beyond IPNs film could act as electron well at the applied voltage above 10 V. © 2000 John Wiley & Sons, Inc. J Appl Polym Sci 75: 721–727, 2000

Key words: dielectric constant; polyurethane/polybutyl-methacrylate interpenetrating polymer networks; capacitance–voltage measurement; metal–insulator–semiconductor structure

INTRODUCTION

The metal–insulator–semiconductor (MIS) structure has been extensively studied in the semiconductor industry and characterized by the properties of the insulator and the semiconductor–insulator interface.[1,2] The capacitance–voltage (C-V) analysis of MIS structure is frequently used to investigate fundamental parameters for MIS devices, such as flatband voltage, interface trap density, threshold voltage, and effective charge density on insulator thin films.[3,4] Besides conventional inorganic insulator film, polymer and electrically conductive polymer films have received much attention recently in the study of the organic/semiconductor heterostructure using the MIS structure.[5]

As far as polymer is concerned, M.Campos et al.[6] have investigated the properties of the junction prepared by depositing a dithienothiophene/dithienopyrrole copolymer (PDTDP) directly onto a n-Si substrate. By using C-V characteristics over a wide temperature range, it was demonstrated that the carrier transport can be understood in terms of a thermionic emission space charge limited current model. L. Zhang et al.[7] used the microgel star-shaped amphiphile (MSA) Langmuir–Blogett (LB) film as the insulator layer within the MIS structure with which the dielectric constant of MSA films was calculated from the high-frequency C-V characteristics. Because of the poor mechanical and thermal stability of LB film, Dewa et al.[8] used polymerized film to study the field effect and thermal stability of MIS structures. Although all the results mentioned

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above are promising, the extensive utilization of organic polymer films as an insulator in MIS devices requires controllable film morphologies, long-term stability, and a better understanding of the physics of organic insulator-semiconductor interface. This target can be reached by testing different chemical compounds and different preparation methods.[9]

Although latex interpenetrating polymer networks (IPNs) and their dielectric properties have been extensively studied,[10–14] little investigation about the dielectric constant using MIS structure has been reported. In this paper, the dielectric constant of polyurethane/polybutyl-methacrylate (PU/PBMA) IPNs was studied using high-frequency C-V characteristics with the Al/IPNs/n-Si structure. The high-frequency C-V properties are analyzed in terms of the standard MIS diode equations. When the applied bias was above 10 V, a plateau was observed in the C-V characteristics in the depletion region, which is different from the standard MIS structures in which the insulator layers were fabricated by conventional polymers such as polystyrene (PSt)[15] and C_{60}-polymer[16] films. This phenomenon was investigated by the electron transport process in the MIS structure, which has the potential application to make memory devices since the charge trapping in the insulator film has long been studied as a mechanism for semiconductor memory and data storage.[17]

EXPERIMENTAL

Materials

Butyl methacrylate (BMA) and styrene supplied by Shanghai Chemical Co. were distilled under reduced pressure before use. Ethylene glyol dimethacrylate (EGDMA) (Aldrich Chemical Co., USA) was used as crosslinker of AB crosslink. Trimethylol propane (TMP) and 1,3-butanediol (1,3-BD) were added as crosslinker and extender of PU chain, respectively. Hydroxyl polybutydiene (HPB), used as polyol, was added as received. Azobis-isobutyronitrile (AIBN) and dibutyltin dilaurate (T-12) were used as radical initiator of BMA and catalyst of PU, respectively. The mixture of ethyl acetate xylenes were used as solvent. The n-type single-crystal silicon (thickness = 6×10^{-2} cm) was made in the Third Semiconductor Devices Factory of Beijing. The density of the carriers in silicon wafer is $5 \times 10^{13} \sim 10^{15}$ cm^{-3}. There was a SiO_2 layer (thickness = 3×10^{-7} cm) on the surface of the single-crystal silicon.

Polymerization of PU/PBMA IPNs and PSt

The PU/PBMA IPNs latex mixture was prepared in a four-neck flask equipped with a nitrogen purge, the stirrer, reflux condenser, and thermometer. The amounts of 11.8 g HPB, 0.13 g TMP, 0.225 g 1,3-BD, and 8 mL xylenes were stirred and gently warmed until these materials were completely dissolved. At the temperature of 323 K, 12.6 g BMA, 0.086 g EGDMA, and 0.059 g AIBN were added and stirred under nitrogen atmosphere. Then the temperature was gradually raised to 353 K and maintained for 2 h. After the prepolymerization of PBMA was complete, the mixture was cooled to 333 K and 0.067 g T-12 catalyst was added with rapid stirring. Finally, the system was standing at 333 K for 1 h and cooled to room temperature. The IPNs based on crosslinked PU and linear PBMA were synthesized. The PSt latex was prepared by emulsion polymerization as the previous report.[18]

Fabrication of the MIS Structure

The silicon wafers were cleaned by detergent, then rinsed by twice-distilled water and then dried before the deposition of the latex. A series predetermined amounts of dilution IPNs solutions and PSt latex were dropped on n-type silicon substrates on which there is a SiO_2 insulator layer. The drop spread over the accessible area encircled by a Teflon ring. The thickness of IPNs film on n-Si were measured by Modle 6TA interference microscopy. After IPNs films were formed on the n-type silicon wafer, an Al electrode [with the main electrode $1/4\pi d^2$, d = 0.4 mm] was deposited on the top of the film by vacuum evaporation at the pressure of 4×10^{-3} Torr using GD-300 high evaporation platting system to form Al/IPNs/Si(MIS) structure. The diagram of its structure and its equivalent circuit are shown in Figure 1.

Measurement of the High-Frequency C-V Characteristics of the MIS Structure

The high-frequency C-V characteristics were measured using an EG&G PAR Model 410 C-V plotter operated at a frequency of 1 MHz at room temperature. The electrode to silicon is an ohmic contact.

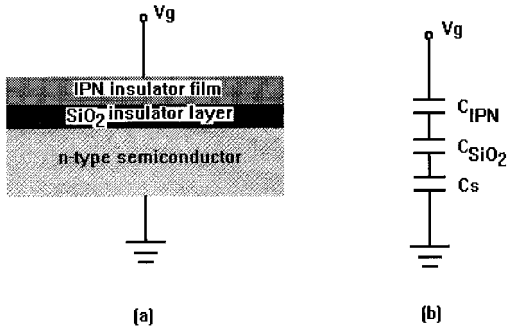

Figure 1 (a) The diagram of the MIS structure using IPNs film on n-Si wafer as the insulator layer. (b) The equivalent circuit of the structure in (a).

RESULTS AND DISCUSSION

Figure 2 shows the high-frequency C-V characteristics of the Al/IPNs/n-Si structure with different insulator layers, in which the accumulation, depletion, and inversion regions could be seen as a typical MIS structure. In curve a, the insulator layer is SiO_2 on the n-Si wafer only, and the C-V characteristics acts as the typical metal–oxide–semiconductor structure.[19] In curve b, the insulator layer is formed by pure PSt latex film and the SiO_2 layer; the C-V characteristics behaves as a typical MIS structure. In the case of curve c, the insulator layer is formed by IPNs latex film and the SiO_2 layer; a plateau in the C-V curve was observed. It is clear that the plateau was caused by IPNs insulator layer.

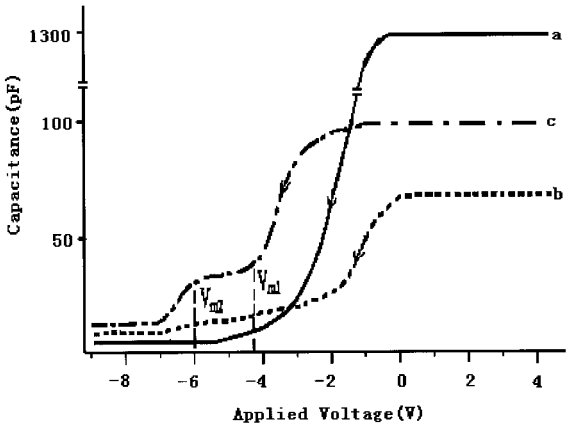

Figure 2 High-frequency C-V characteristics of the Al/IPN/n-Si structure with different insulator layers. (a) Insulator layer is SiO_2 only (b) insulator layer is PSt latex film and SiO_2 film (c) insulator layer is IPNs film and SiO_2 film. (Sweep voltage: 100 mV/s; bias: V_g = 10 V.)

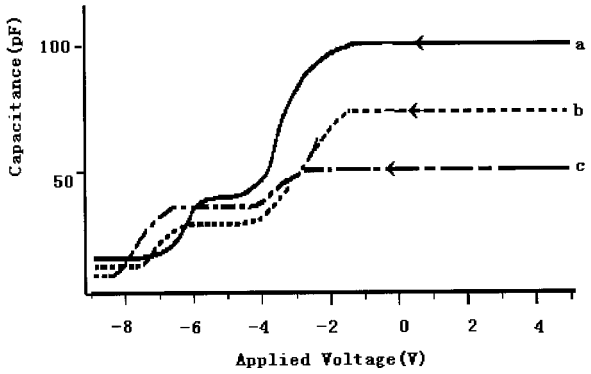

Figure 3 The high-frequency C-V characteristics of the Al/IPNs/n-Si structure with different thickness of IPNs film at the bias V_g = 10 V. (a) d_{IPN} = 40 nm; (b) d_{IPN} = 55 nm; (c) d_{IPN} = 78 nm. (Sweep voltage: 100 mV/s; bias: V_g = 10 V.)

Figure 3 shows the higher frequency C-V characteristics of the Al/IPNs/n-Si structure with different thickness of IPNs film at the bias V_g = 10 V. In the accumulation region, the total capacitance decreases with the increasing of IPNs film thickness, which is in very good agreement with the result reported by L. Zhang et al.[7] in the study of the Al/MAS/n-Si structure. When the MAS LB film increases from one layer to thirteen, the total capacitance decreases from about 200 to 100 pF.

In the accumulation region, the value of the capacitance of single-crystal silicon is zero, so the insulator capacitance can be expressed as follows according to Figure 1(b) when the SiO_2 layer on the silicon surface is taken into account:

$$\frac{1}{C} = \frac{1}{C_{SiO_2}} + \frac{1}{C_{IPN}} + \frac{1}{C_S} \tag{1}$$

$$C_{SiO_2} = \frac{\varepsilon_{SiO_2}\varepsilon_0 A}{d_{SiO_2}} \tag{2}$$

$$C_{IPN} = \frac{\varepsilon_{IPN}\varepsilon_0 A}{d_{IPN}} \tag{3}$$

$$C_S = \frac{\varepsilon_S}{W} \tag{4}$$

where $\varepsilon_0(8.854 \times 10^{-12}$ F/m) is the free-space permittivity, ε_{SiO2} and ε_{IPN} are the dielectric constants of the SiO_2 layer and IPNs layer, and d_{SiO2} and d_{IPN} are the thickness of the SiO_2 layer and IPNs film layer, respectively. C and C_s are the

Table I The Experimental Values of the Insulator Capacitance with Different Thickness of IPN Films of the Al/IPNs/n-Si Structure[a]

Film thickness d_{IPN} ($\times 10^{-10}$ m)	400	456	550	640	780
Insulator capacitance C ($\times 10^{-12}$ F)	105	90	80	70	55
Reciprocal insulator capacitance C ($\times 10^{9}$ F^{-1})	9.52	11.11	12.5	14.29	18.18

[a] $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m; $A = 1.256 \times 10^{-7}$ m^2.

total capacitance and the semiconductor depletion-layer capacitance respectively, C_{SiO2} and C_{IPN} are the insulator capacitance of the SiO2 layer and IPNs film. W is the depletion width of the silicon substrate, and $A(1.256 \times 10^{-7}$ $m^2)$ is the area of the top electrode in the Al/IPNs/n-Si structure.

According to equations (1–3), the insulator capacitance can be expressed as follows:

$$\frac{1}{C} = \left(\frac{d_{SiO_2}}{\varepsilon_{SiO_2}} + \frac{d_{IPN}}{\varepsilon_{IPN}}\right)\frac{1}{\varepsilon_0 A} \tag{5}$$

The experimental values of the reciprocal capacitance with different thicknesses of IPNs films are shown in Table I. The reciprocal capacitance are linear with respect to the thickness of IPNs film as shown in Figure 4. The equation of the line in Figure 4 can be expressed as

$$\frac{1}{C} = 7.348 \times 10^8 + 2.19 \times 10^{17} d_{IPN} \tag{6}$$

On the value of the slope and the intercept of the straight line, one can get

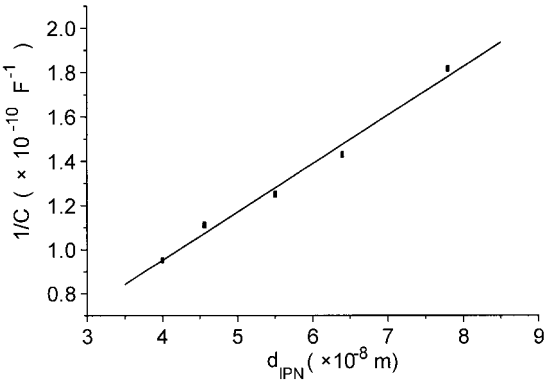

Figure 4 The relationship of reciprocal insulator capacitance versus the thickness of IPNs film layer.

$$\frac{d_{IPN}}{\varepsilon_{IPN}} \cdot \frac{1}{\varepsilon_0 A} = 2.19 \times 10^{17} \tag{7}$$

$$\frac{d_{SiO_2}}{\varepsilon_{SiO_2}} \cdot \frac{1}{\varepsilon_0 A} = 7.348 \times 10^8 \tag{8}$$

From eqs. (7) and (8), the dielectric constants of IPNs and SiO_2 using $d = 3.0$ nm for its thickness were 4.1 and 3.67, respectively. In order to compare the value of the dielectric constant with that of other materials, the dielectric constants of others for several MIS structures are shown in Table II. The $\varepsilon_{IPN} = 4.1$ and $\varepsilon_{SiO2} = 3.67$ obtained in this work were in good agreement with the available literature values.[7,9,16,20,21]

Figure 5 shows the high-frequency C-V characteristics of the Al/IPNs/n-Si structure with different applied voltage. The insulator capacitance has an increment in the accumulation region, while the minimum capacitance decreases in the inversion region with the increasing of applied voltage. In the depletion region, the C-V characteristics acts as a typical MIS structure when the applied voltage is below 5 V, but when the applied voltage is above 10 V, a plateau that indicates $dC/dV = 0$ appears. This phenomenon was first observed as far as we know when the insulator layer is formed by the polymer or copolymer in the MIS structure. This behavior can be understood

Table II Values of the Dielectric Constants of Other Materials Used as Insulator Layer in Different MIS Structures

Sample	ε	Reference
Au/Cadmium stearate/InP	2.52	20
Au/C_{60}-polymer/p-Si	4.6	16
Al/MSA LB film/n-Si	2.27	7
Ag/PPAF/ITO	3.57	22
Al/SiO_2/n-Si	3.9	9
	3.67	This work
Al/IPNs/n-Si	4.1	This work

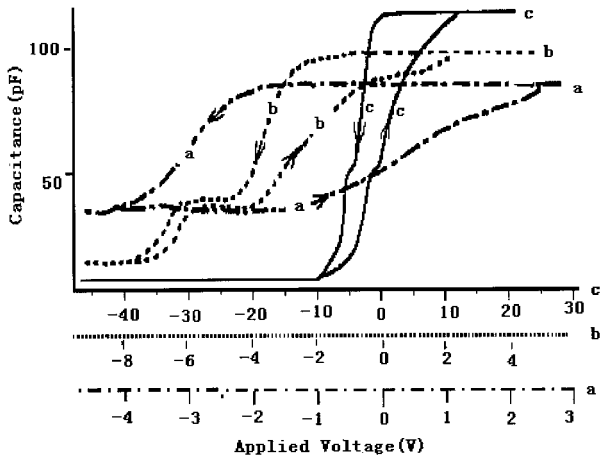

Figure 5 The high-frequency C-V characteristics of the Al/IPNs/n-Si structure with different applied voltage. (a) V_g = 5 V; (b) V_g = 10 V; (c) V_g = 50 V. (Sweep voltage: 100 mV/s; film thickness: 40 nm.)

by the carrier transportation in the insulator layer.

In an ideal MIS structure the conductivity of the insulator film is assumed to zero, but real insulator films show carrier conduction when the electric field is sufficiently high. Under biasing condition, the electric field in an insulator can be expressed by[22]

$$E_{\mathrm{IPN}} = E_s\left(\frac{\varepsilon_s}{\varepsilon_{\mathrm{IPN}}}\right) \tag{9}$$

where E_{IPN} and E_{s} are the electric field in the insulator and the semiconductor respectively, and ϵ_{IPN} and ϵ_{s} are the corresponding permittivity.

Under high electric field in the insulator layer, a field-controlled electron transport mechanism such as tunneling or internal hopping are possible. This tunneling effect extensively depends on the applied bias on the MIS structure, the thickness of the IPNs film, and the area of the top electrode. Within the IPNs film, many unsaturated bands (—C=C—) act as the electron well beyond the MIS structure.

According to the report of Clark and Feast,[23] the polymer and copolymer can be considered as a semiconductor with a large band gap; we can get the diagram of the conductive band energy level of the Al/IPNs/n-Si structure at a different applied bias, which is shown in Figure 6. In the accumulation region [Fig. 6(a)], a large positive bias attracts electrons to the silicon surface and the silicon bands bend down. As the positive bias decreases, surface electron density will decrease, making C_{s} smaller when surface potential decreases to zero, and the flatband condition is achieved [Fig. 6(b)].

In the depletion region, with a certain lower negative bias, the electrons on the metal surface cannot penetrate the insulator barrier layers to the electron well before a threshold (V_{m1}) because of a relatively lower electric field on the IPNs film. The capacitance C_{IPN} and C_{s} are given by eqs. (3) and (4) respectively, and the differential capacitance (C) decreases with the increasing negative applied bias. When the applied voltage increases to the threshold (V_{m1}), the electric field is high enough to make electrons on the metal surface penetrate to the electron well of the IPNs film [Fig. 6(c)]. Because the electrons are stored in the electron well in IPNs film, the hole generation in the depletion region is stopped and the depletion width is no longer changed. The depletion capacitance of silicon (C_{s}) keeps the unchanged value until the electrons cannot be stored and begin to penetrate the SiO_2 layer to the silicon substrate at another threshold voltage (V_{m2}). During the period of the voltage from V_{m1} to V_{m2}, the electrons are trapped into the electron well and the space charge width and the space charge capacitance (C_{s}) are to be constant. The electrons stored in the IPNs film behave as the fixed negative charges, which makes the C-V curves shift toward more positive direction in the reverse scan. This is why a plateau and the hysteresis could be observed in the C-V properties. The plateau effect in the high-frequency C-V characteristics was also studied by K. Kreher[24] and our previous work[15] in

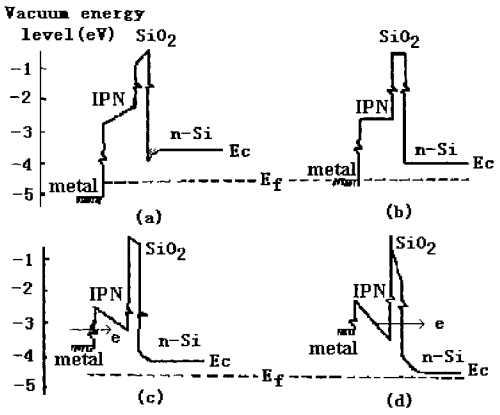

Figure 6 The diagram of the conductive band energy level model of the Al/IPNs/n-Si structure at different applied bias. (a) Positive bias; (b) flatband condition; (c) negative bias; (d) more negative bias.

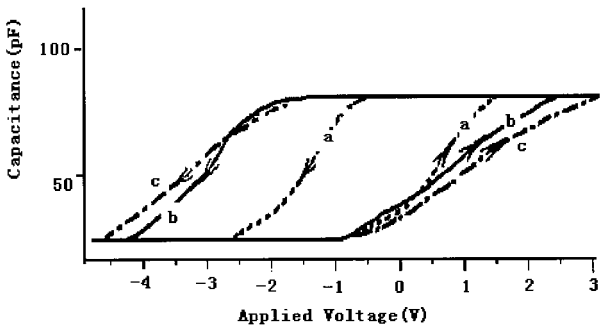

Figure 7 The C-V characteristics of the Al/IPNs/n-Si structure with different voltage scan rates. (a) 5 mV/s; (b) 100 mV/s; (c) 500 mV/s. (Bias: V_g = 5 V; film thickness: 40 nm.)

InP/$Ga_{0.47}In_{0.53}$/InP and Al/polymer-Fe_2O_3-polymer/n-Si structures respectively, which can be used to detect the presence or absence of the charges stored in the insulator layer of the MIS structure.[25]

After the applied bias at V_{m2}, the electrons from the metal surface penetrate the insulator layer to the silicon surface directly and the hole generation is again controlled by the applied bias. In the inversion region [Fig. 6(d)], the applied voltage is made even more negative, surface hole density exceeds surface electron density, but the minority carrier (hole) generation is much smaller at higher frequency, and the capacitance in inversion region is only dependent on minority carriers in depletion while the width reaches the maximum value, which makes the total capacitance to minimum.

Figure 7 shows the C-V characteristics of the Al/IPNs/n-Si structure with different voltage scan rates. The hysteresis was observed in ally cases; moreover, the faster the scan rate, the more severe is the hysteresis. As it is well known, the hysteresis in the C-V curves is due to interface state recharge.[26] So, the motion of charges in the insulator layer should play a major role in this hysteresis effect.[27] The interface charges located at the insulator/Si interface can exchange charges with silicon, but the rate is low enough to follow the sweep voltage. Under a high voltage scan rate, it is more difficult for the charges on the silicon surface to neutralize the fixed positive charges on SiO_2 film, so the positive charges in the insulator layer is relatively larger. Because the positive charges in the insulator layer makes the C-V curves shift to more a negative direction, it is not surprising that the C-V curve under a high voltage scan rate [Fig. 7(b, left)] is located at the left of the curve under slow sweep voltage [Fig. 7(a, left)] in the scan direction from positive to negative (counterclockwise). When the scan direction changes from counterclockwise to clockwise, the stored negative charges may make the curve to shift to a more positive direction under high sweep voltage (Fig. 7, right).

CONCLUSION

In this paper, the IPNs latex film was used as insulator layer to fabricate the Al/IPNs/n-Si structure and the high-frequency C-V characteristics of the structure was performed under room temperature. The dielectric constants ϵ_{IPN} = 4.1 and ϵ_{SiO2} = 3.67 were obtained using the insulator capacitance in the accumulation region of the C-V curves. In the C-V curves, a plateau was observed in the depletion region when the applied voltage is above 10 V and an increased hysteresis was also observed at high sweep voltage. The plateau in the C-V curves of the Al/IPNs/n-Si structure demonstrated that the unsaturated bonds beyond IPNs film can store electrons under a certain applied voltage, which showed a new potential application of IPNs and could give us a new material in the study of semiconductor memory devices. Except for the effect of the insulator/Si interface states, that the electrons stored in the IPNs film act as the fixed negative charges also makes us to get an increased hysteresis in the Al/IPNs/n-Si structure.

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REFERENCES

1. Passlack, M.; Hong, M.; Mannaerts, J. P. Solid State Electronics 1996, 39(8), 1133.
2. Landheer, D.; Yousefi, G. H.; Webb, J. B. J Appl Phys 1994, 75, 3516.
3. Chattopadhyay, P. Solid State Electronics 1996, 39(10), 1491.
4. Koukab, A.; Bath, A.; Losson, E. Solid State Electronics 1997, 41(4), 635.
5. Jung, J. W.; Lee, H. C.; Wang, J. S. Thin Solid Films 1996, 290–291, 18.
6. Campos, M.; Miceli, G. C.; Camaioni, N. J Phys D Appl Phys 1995, 28, 2123.

7. Zhang, L.; Zhu, M.; Liu, Z. X.; Shen, J. C.; Bai, Y. B.; Li, T. J. Chem J Chinese Universities 1995, 16, 167.
8. Dewa, A. S.; Fung, C. D.; Dipoto, E. P.; Richert, S. E. Thin Solid Films 1985, 132, 27.
9. Shen, Y.; Boragno, C.; Rolandi, R.; Valbusa, U. Thin Solid Films 1990, 187, 155.
10. Wang, J. Y.; Liu, R. Y.; Li, W. H.; Li, Y. W.; Tang, X. Y. Polym Intl 1996, 39,101.
11. Cai, Y. L.; Jiang, Z. M.; Yang, D. F.; Liu, P. S. J Appl Polym Sci 1998, 68, 1689.
12. Pan, J. P.; Shiau, G. Y.; Chen, K. M. J Appl Polym Sci 1992, 44, 467.
13. Karabanova, L.; Pissis, P.; Kanapitsas, A.; Lutsyk, E. J Appl Polym Sci 1998, 68, 161.
14. Kyritsis, A.; Pissis, P.; Grammatikakis, J. J Polym Sci Polym Phys 1995, 33, 1737.
15. Qian, X. M.; Du, H.; Zhang, X. T.; Bai, Y. B.; Li, T. J.; Tang, X. Y.; et al. Supramol Sci 1998, 5, 683.
16. Guan, Y. G.; Dai, G. R. Acta Scientiarum Naturalium Universitatis Jilinensis 1996, 3, 56.
17. Barrett, R. C.; Quate, C. F. Ultramicroscopy 1992, 42, 262.
18. Du, H.; Zhang, P.; Liu, F.; Kan, S.; Wang, D.; Li, T.; Tang, X. Polym Intl 1997, 43, 274.
19. Nicollian, E. H.; Brews, J. R. MOS (Metal Oxide Semiconductor) Physics and Technology; Wiley—Interscience: New York, 1982; p 99–174.
20. Roberts, G. G.; Vincett, P. S.; Barlow, W. A. J Phys Chem 1978, 11, 2077.
21. Sharma, G. D.; Sandogaker, S. G.; Roy, M. S. Thin Solid Films 1996, 278, 129.
22. Sze, S. M. Physics of Semiconductor Devices, 2nd ed.; Wiley—Interscience: New York, 1981; p 402.
23. Fabish, T. J.; Duke, C. B. Polymer Surface; Wiley—Interscience: New York, 1978; chap 4.
24. Kreher, K. Phys Stat Sol A 1993, 135, 597.
25. Kan, S.; Yu, S.; Peng, X.; Zhang, X.; Li, T. J. Colloid Interface Sci 1996, 178, 673.
26. Kaplan, G. Solid State Electronics 1981,24, 87.
27. Koukab, A.; Bath, A.; Losson, E. Solid State Electronics 1997, 41(4), 635.